

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Nui Chong; Aaron Rogers; Kerry Ilgenstein  
Assignee: Lattice Semiconductor Corporation  
Title: Electrostatic Discharge Protection Circuits  
Serial No.: Unknown Filing Date: Herewith  
Examiner: Unassigned Group Art Unit: Unknown  
Docket No.: M-15338 US

Irvine, California  
March 24, 2004

COMMISSIONER FOR PATENTS  
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

UNDER 37 C.F.R. §1.97 AND § 1.98

Dear Sir:

Pursuant to 37 C.F.R. §1.97 and §1.98, Applicant calls the following documents (copies enclosed) to the attention of the Examiner. It is respectfully requested that the cited references be expressly considered during the prosecution of this application, and the references be made of record therein and appear among the "references cited" on any patent to issue therefrom. Note that U.S. patent application nos. 10/664,170 and 10/769,174 are being submitted for the Examiner to consider regarding double patenting.

A PTO form 1449 listing these documents is enclosed.

Citation of the above documents shall not be construed as:

1. an admission that the documents are necessarily prior art with respect to the instant invention;

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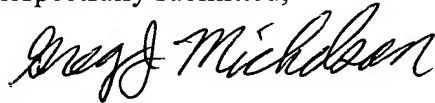
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2. a representation that a search has been made, or
3. an admission that the information cited herein is, or is considered to be material to patentability as defined in §1.56(b).

Applicant(s) believes that no fee is required for submission of this statement. However, if a fee is required, the Commissioner is authorized to deduct such fee from the undersigned's Deposit Account No. 50-2257. Please deduct any additional fees from, or credit any overpayment to the above-noted Deposit Account.

Express Mail #EV252525738US

Respectfully submitted,



Greg J. Michelson  
Attorney for Applicant(s)  
Reg. No. 44,940

U.S. Department of Commerce, Patent and Trademark Office					Atty Docket No.		Serial No.	
					M-15338 US		Not yet assigned	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT					Applicant(s)			
(Use several sheets if necessary)					Nui Chong; Aaron Rogers; Kerry Ilgenstein			
					Filing Date		Group	
					Herewith		Not yet assigned	
U.S. Patent Documents								
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate	
	AA	6,028,758	02/22/2000	Sharpe-Geisler				
	AB	6,091,595	07/18/2000	Sharpe-Geisler				
	AC							
	AD							
	AE							
	AF							
	AG							
	AH							
	AI							
	AJ							
	AK							
Foreign Patent Documents								
							Translation	
		Document	Date	Country	Class	Subclass	Yes	No
	AL							
	AM							
	AN							
	AO							
	AP							
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)								
	AQ	ESD Protection For Mixed-Voltage I/O Using NMOS Transistors Stacked In A Cascode Configuration, by Warren R. Anderson et al., Digital Equipment Corporation, Shrewsbury, MA 01545						
	AR	U.S. patent application serial number 10/664,170, filed on 09/16/2003, entitled "Electrostatic Discharge Protection"						
	AS	U.S. patent application serial number 10/769,174, filed on 01/29/2004, entitled "Electrostatic Discharge Simulation"						
Examiner			Date Considered					
<p>*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.</p>								